Layout and DRC

ECE 09414 - 2 VLSI

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I. Introduction

The purpose of this lab procedure was to learn about setting up the layout for a given circuit. In this instance the layout for an inverter was created as to show how the inverter would be printed onto a chip for physical use. This allows for a greater understanding of how these circuits are printed and how designers create these layouts.

II. Procedure

Using the previously created inverter as a template for the layout design a new cell view was created in order to create the layout. The pmos and nmos were both created by denoting the pactive and nactive regions. These regions were then given an input with the addition of a poly layer and were give contacts on each of the pactive and nactive regions. These contacts were used to connect the drain of the pmos to the drain of the nmos with metal1. The contacts were also used to connect the circuit to VDD and ground. After the pmos was completed the nwell was placed around it. The metal that connected the drain of the pmos to the drain of the nmos was connected by a path of metal1 and the poly input was also connected to a separate input contact by a path of poly. Once the layout was complete the DRC was ran to ensure the layout had no flaws.

III. Results

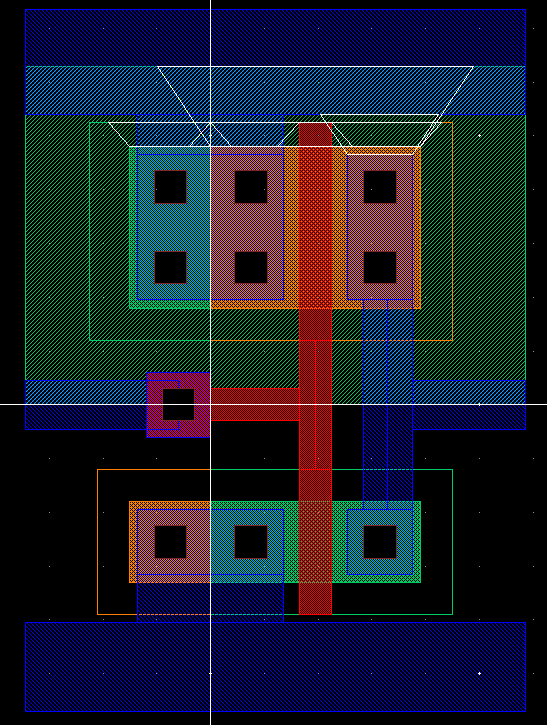


Figure 1: The completed layout of the inverter. Metal1 being denoted by the blue area when the drain of the pmos is connected to the drain of the nmos. This metal layer also shows that the circuit will be connected to VDD, ground, and an input. The nwell is in place around the pmos and the poly allows for the input to reach both the pmos and the nmos.

IV. Conclusions

From the layout created it can be seen that the inverter will work once it is printed onto a physical chip for practical use. When following the design rules for the layout of a circuit it can be relatively easy for a circuit to continue passed theoretical design and be pushed into physical design and use. Taking this process beyond a single inverter could create a much more complex and difficult layout design.